iND80001 “Lodestar”

indie’s ultra-integrated USB 3.1 type-C cable marker (E-marker) chip.

12/10/2015 **Preliminary Data sheet**

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4.0 GENERAL DESCRIPTION

The iND80001 is a complete low cost, single chip cable marker for USB PD Type-C (baseband) cables. With low silicon area and just 4 IOs the device is designed exclusively for very high volume Type-C cables with basic marker requirements.

4.1 KEY FEATURES

- USB PD 2.0 compliant.
- USB Type-C 1.0 compliant
- Single chip solution.
- 4 pin package.
- PROM programmed through vendor message protocol.
- Based on Obsidian Technology's mature PD technology.
- Integrated PROM enables customized response to a wide range of vendor requirements.
- Power <5mW. Enabled by CC data activity. I.e. very low duty cycle.
- Programming can be done after assembly into the cable.
- Fuse lock function.
- Supports low cost 4 layer PCB assembly.
- Supported with module level test program.
- Package options: WLCSP4, DFN6
- CC high impedance when powered down.
- IEC61000-4-2 4kV ESD protection

4.2 MAIN FUNCTIONS & SYSTEM OVERVIEW

Physical Layer.

- Based on Obsidian's OTC9107 port chip physical layer, this provides CC line driving and reception without external components. It includes data slicer, activity detection, voltage level detection, and slew rate controlled driver.

LDO.

- Provides bandgap, and internal voltage regulation for the logic the physical layers. Power diodes also provide the required power isolation between two possible power sources (one at each end of the cable).

Oscillator.

- A low temperature drift 12MHz oscillator provides logic clocking when required. The provided test program automatically trims the oscillator during test for an overall frequency accuracy of ±5%.

Protocol Engine.

- Implements the low level protocol and logic PHY functions required by the standard, such as CRC generation and testing, 4b5b coding, BMC coding, clock recovery, and SERDES.

Marker State Machine.

- Provides the subset of device functions required to recognize vendor messages and return responses based on PROM data.

Programmed response will respond with Cert-Stat VDO and Cable-VDO with all relevant fields programmable.

Programming Board is available.

Supporting Software in C form is available for rapid implementation of production test.

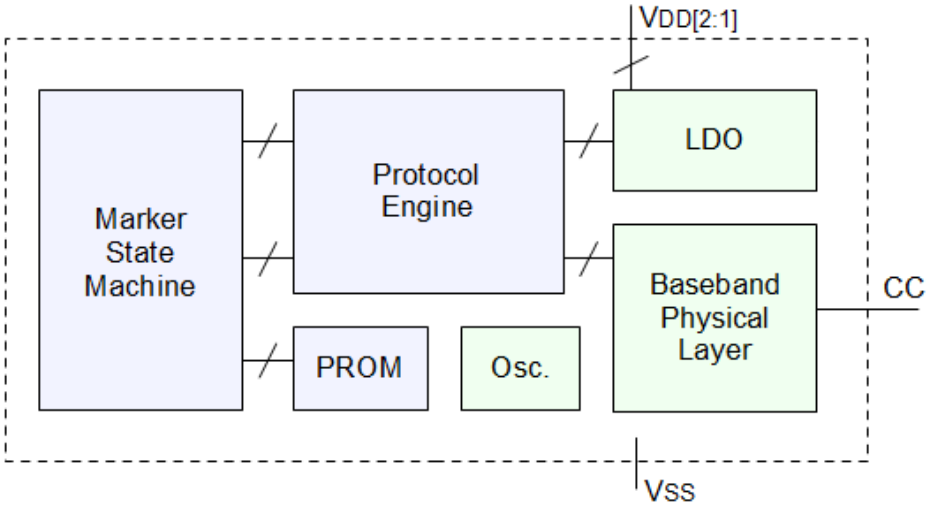


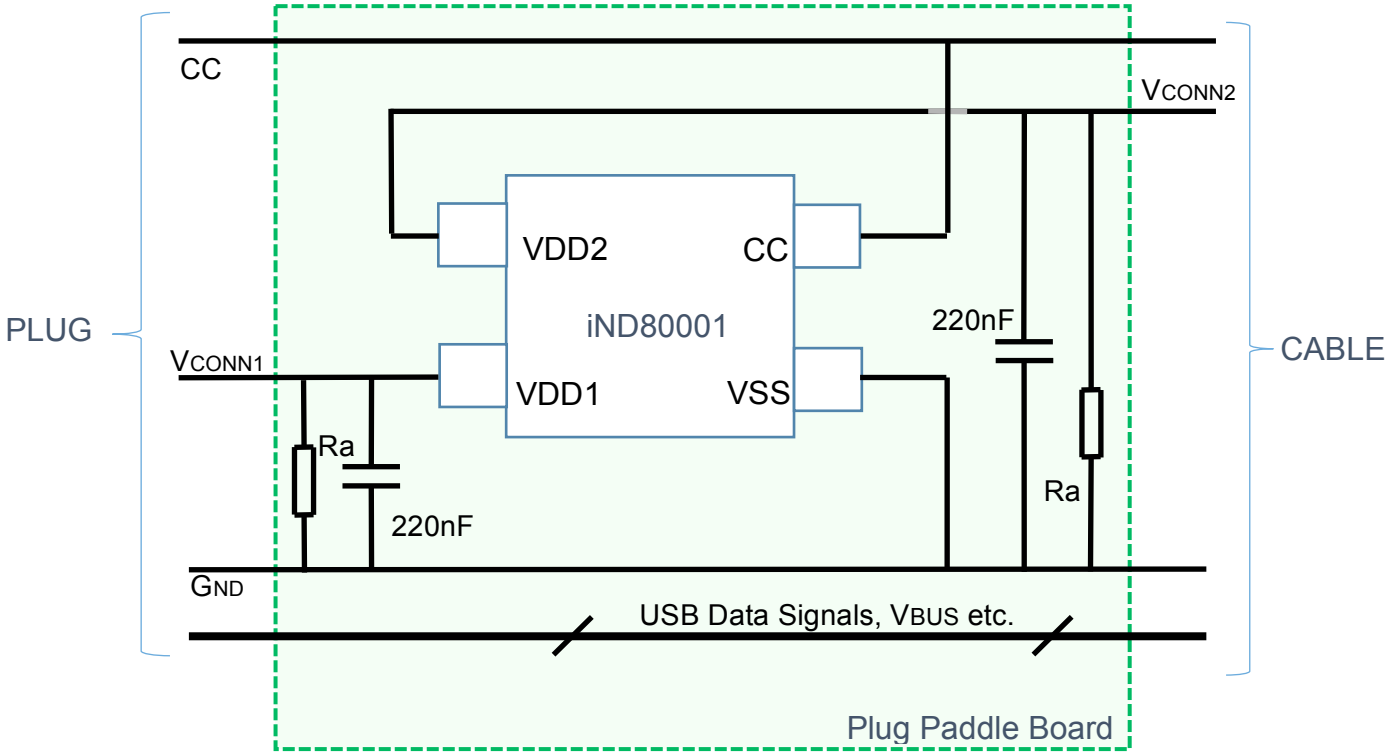
Figure 1 iND80001 Block Diagram

4.3 APPLICATION DIAGRAM

The iND8001 is a single chip marker that requires only the VDD and VSS pins to be decoupled by external capacitors. 16V 220nF ceramic types are recommended.

The applications diagram shows a typical arrangement for single chip per cable. However, it is also possible to fit the plug at both ends with an identical chip, and avoid needing to provide a VCONN conductor through the cable. This is more cost effective for long cables.

Figure 2 iND80001 Application Diagram



5.0 ELECTRICAL CHARACTERISTICS

5.1 ABSOLUTE MAXIMUM RATINGS

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 1 Absolute Maximum Ratings

Parameter	Rating
Maximum voltage range on VDD1, VDD2, or CC Vs VSS	-0.75 - 6V
Junction temperature range	-65°C – 150°C
Storage temperature range	-65°C – 150°C
CC pin short circuit time	Indefinite

5.2 OPERATING CONDITIONS

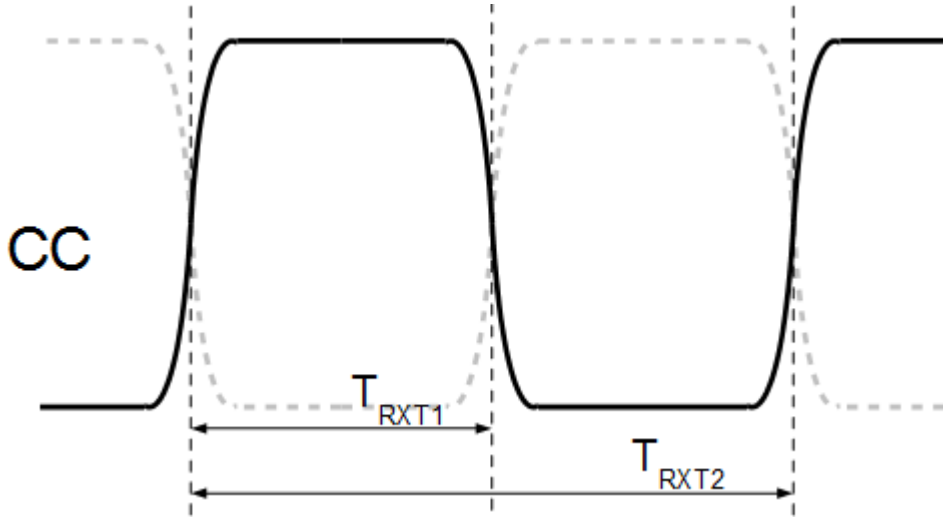


Figure 3 BMC “1” Receive Bit Timing

Table 2 Operating Conditions

Measured at T_A = 25°C, V_{DD} = 5V unless otherwise started.

Parameter	Condition	Min	Typ	Max	Units
Operating Voltage V_O	Max(V_{DD1},V_{DD2})	4.5	5	5.5	V
Operating Temperature T_O		-40		125	°C
Idle current I_{IDL}	Current into V_{DD1} + V_{DD2} with no CC bus activity		55		µA
Transmit current I_{TX}	Mean current into V_{DD1} + V_{DD2} during transmit		900		µA
Receive current I_{RX}	Mean current into V_{DD1} + V_{DD2} during packet receive		150		µA
Receive lock time T_{RXL}	First CC edge to good received edge			18	µS
Receive BMC "1" centre bit edge timing window T_{RXT1}.	CC 1ST UI edge to "1" edge if present	1.2		2.03	µS
Receive BMC end of bit window T_{RXT2}.	CC 1ST UI edge to end of bit edge	2.6		4.0	µS
Clock off time T_{CKO}	Last CC edge to clock off	50		200	µS
Transmit drive high voltage V_{TH}	CC load 0 – 1.2nF, or open transmission line over T_{RNG}	1.0	1.1	1.2	V
Transmit drive low voltage V_{TL}	CC load 0 – 1.2nF, or open transmission line over T_{RNG}	0		0.1	V
Transmit driver rise/fall T_{TRF} (Trimmed during test)	CC load 0 – 1.2nF, or open transmission line	200	300	500	nS
Transmitter Unit Interval Time T_{TUI} (Trimmed during test)	CC pin, typical load	1.5	1.66	1.83	µS
Oscillator temperature drift	-40°C – 125°C			2	%
CC pin impedance Z_{CC}	0V < V_{CC} < 5V		1		MΩ

6.0 PROGRAMMING

6.1 MESSAGES SUPPORTED

The iND80001 supports baseband messages required for basic Type-C cable markers as follows:

Table 3 Type-C message

PD Message type	Code	Action
Soft Reset	1101	Normal Soft Reset, reset ID-counter and discard any message waiting to be sent.
BIST	0011/0101	Can turn on BIST mode 2.
Vendor Defined	1111	See table below.
Private Programming	0000	Intended to program the chip before being taken into use. See Table 5 Programming Commands below.

A GoodCRC message will not be answered.

Any message except those in the table above will be ignored after being acknowledged.

6.2 VDM COMMAND OVERVIEW

Table 4 VDM Command Overview

Structured VDM Command	Command	Action
Any unstructured VDM	NA	Ignored
Discover Identity	1	ACK with response
Discover SVIDs	2	NAK
Discover Modes	3	NAK
Enter Mode	4	NAK
Exit Mode	5	ACK no further response
Attention	6	NAK
Any other code		NAK

6.3 PROGRAMMING

- Programming is done by sending messages with header message code "0000". This is a reserved code. Once programming is finished and the locking fuse has been blown, the command will be completely ignored.
- Each programming command carries a PDO of 32 bits as data. This data block is split into 8 bits of command (8 MSB's) and 24 bits of data (24 LSB's). The following table shows how the commands are structured.

Table 5 Programming Commands

Name	bit 31-28	bit 27-24	Action
Test	0x0	Tst[3:0]	For device test only. Note transition of txt[0] to 1 initiates a power on burst. Other combinations are static
Copy	0x1	Address of fuse group (see below)	Copy data from message b23-0 to the group address indicated in bits 27-24to the address indicated in bits 27-24
Burn	0x2	X	Start programming of fuses
Arm	0x4	X	Arm the final fuse
Final	0x8	X	Program final fuse

Any combination of bits 31-28 not mentioned in table is a NOP.

Programming of the content will follow this sequence:

- Copy (23-0) address 0
- Copy (47-24) address 1
- Copy (71-48) address 2
- Copy (95-72) address 3
- Copy (119-96) address 4
- Copy (126-120) address 5

<at this time the responses from the Marker chip will be the same as after burning>

- Burn
- Wait 100 mS
- Arm
- Final

<Note: The Arm and Final must follow directly any other message to command "0000" will disarm>

7.0 FUSE MAP

In the tables below each bit in the VDOs are mapped to corresponding fuses.

7.1 ID VDM

Table 6 ID VDM

Bit(s)	Description	Fuses	Coding
31	Data Capable as USB Host: - Shall be set to one if the product is capable of enumerating USB Devices. - Shall be set to zero otherwise.	105	0
30	Data Capable as a USB Device: - Shall be set to one if the product is capable of enumerating as a USB Device. - Shall be set to zero otherwise.	104	0
29:27	Product Type: - 011b – Passive Cable - 100b – Active Cable	103:101	0 -> ”011” 1-> ”100”
26	Modal Operation Supported:- Shall be set to one if the product supports Modal Operation. - Shall be set to zero otherwise.	100	0
25:16	Reserved. Set to zero.		
15:0	16-bit unsigned integer. USB Vendor ID.	99:84	TID

7.2 CERT STAT VDM

Table 7 Cert Stat VDM

Bit(s)	Description	Fuses	Coding
31:20	Reserved. Shall be set to zero.		
15:0	20-bit unsigned integer.	83:64	TID

7.3 PRODUCT VDO

Table 8 Product VDO

Bit(s)	Description	Fuses
31:16	USB Product ID	63:48
15:0	bcdDevice	47:32

7.4 CABLE VDO

Table 9 Cable VDO

Bit(s)	Description	Fuse(s)
31:28	Cable HW Version	31:28
27:24	Cable Firmware Version	27:24
23:20	Reserved	23:20
19:18	Type-C to Type-A, B, or C	19:18
17	Type-C to Plug/Receptacle	17
16:13	Cable Latency	16:13
12:11	Cable Termination Type	12:11
10	SSTX1 Directionality Support	10
9	SSTX2 Directionality Support	9
8	SSRX1 Directionality Support	8
7	SSRX2 Directionality Support	7
6:5	VBUS Current Handling Capability	6:5
4	VBUS through cable	4
3	SOP” controller present?	3
2:0	USB Superspeed Signaling Support: 00 -> ”000” - USB 2.0 only 01 -> ”001” - USB 3.1 Gen 1 10 -> ”010” - USB 3.1 Gen 1 & 2 11 -> ”011” - Reserved	2:0

7.5 ANALOG TRIMMING FUSES

Table 10 Analog Trimming Fuses

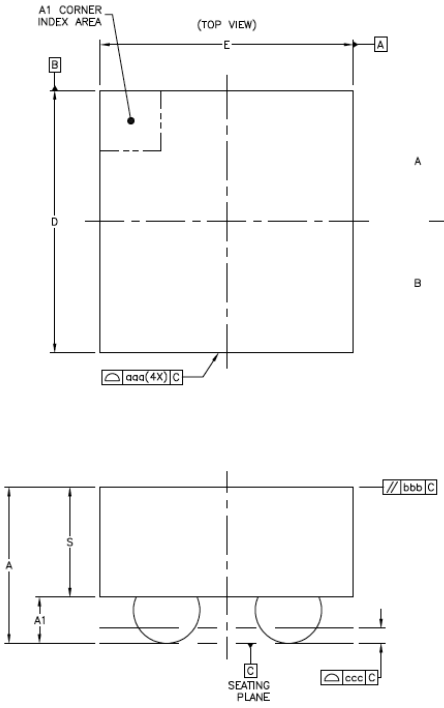
Name	Description	Fuse(s)
ftrim[3:0]	Trim for on chip oscillator (inverted)	115:112
range	Range bit for oscillator. aka ftrim[4]	116
bgvtrm[2:0]	Bandgap voltage trim	119:117
bgitrm[1:0]	bandgap IPTAT current output trim	121:120
itrim[1:0]	Current reference trim	123:122
spare	Unused fuse	124
rtrim[1:0]	Trim for driver rise and fall times	126:125

8.0 PACKAGING OPTIONS

8.1 WLCSP-4 PACKAGE

The WLCSP-4 package option has 4 balls with 400µ pitch. Package size is 800µ × 800µ.

WLCCSP version does not require a CAP pin. Balls are shown on the reverse (down) side of the package. Drawing not to scale.



		SYMBOL	COMMON DIMENSIONS
TOTAL THICKNESS		A	0.512 ± 0.055
WAFER THICKNESS		S	0.36 ± 0.025
STAND OFF		A1	0.122 ~ 0.182
FILM THICKNESS		A2	--- ± ---
BODY SIZE	X	E	0.83
	Y	D	0.861
BALL/BUMP PITCH	X	SE	--- BSC
	Y	SD	--- BSC
EDGE BALL CENTER TO CENTER	X	E1	0.4 BSC
	Y	D1	0.4 BSC
PITCH		e	0.4 BSC
BALL DIAMETER (SIZE)			0.2
BALL/BUMP WIDTH		b	0.188 ~ 0.248
BALL/BUMP COUNT		n	4
PACKAGE EDGE TOLERANCE		aaa	0.03
WAFER FLATNESS		bbb	0.06
COPLANARITY		ccc	0.05
BALL/BUMP OFFSET (PACKAGE)		ddd	0.015
BALL ALLOY			SAC405

Figure 4 WLCSP 4 package drawing

- **Font size tolerance:** (+/- 0.05mm)
- **Marking shift tolerance:** (+/- 0.15mm)

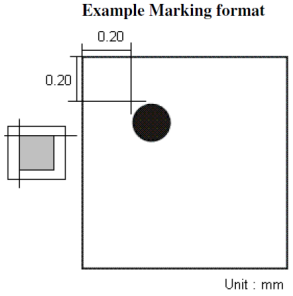


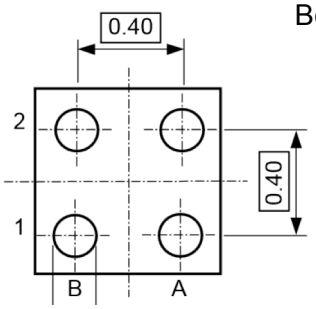
Figure 5 A1 marker

Notes:

- Index is a dot marker referring to pin A1 position
- There are no other marking on the package top

Table 11 WLCSP Pin assignments

Pin	Name
A1	VDD1 / VCONN 1 (0)
B1	VSS
A2	VDD2 / VCONN 2 (1)
B2	CC



Bottom view – A1 dot marker

Note:

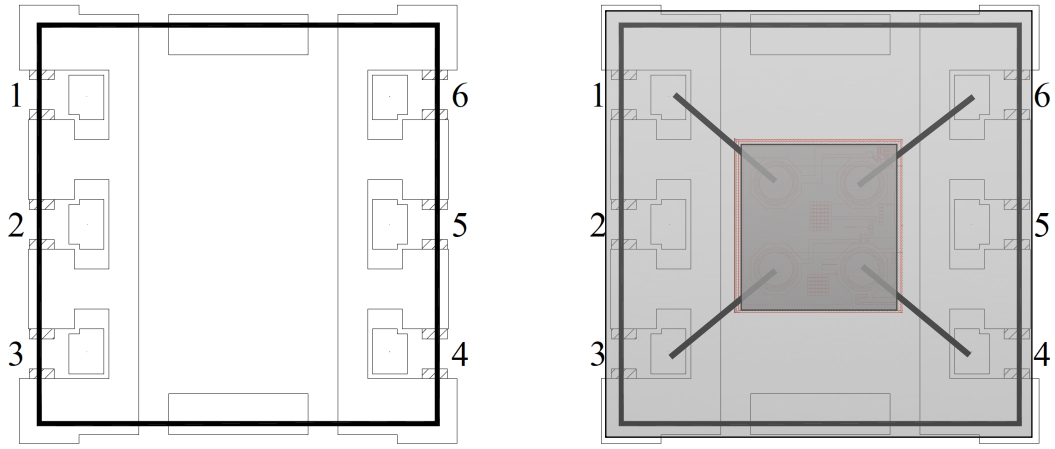
- Power supply VDD1 and VDD2 being interchangeable, they can be referred to as VCONN (1, and 2 - or possibly 0 and 1)

Figure 6 WLCSP 4 marker position in Tape an Reel

8.2 DFN-6 PACKAGE

Indie can also support a DFN 6-lead package in a small 2x2 form factor. The DFN-6 package drawing and dimensions are shown on Figure 7.

Figure 7 DFN-6 2x2 package TOP View and Bonding Diagram



ALL LEADS AND PADS MUST BE WIRED EXCEPT ✱ OR X PLEASE INDICATE THE DIE MARK OR LOGO LOCATION		DIE ID	----	PART NUMBER	0006SN001F05K	
CUSTOMER	----	WIRE AMOUNT		PKG TYPE	SON	
CUSTOMER B/D NO.		PAD TO PAD WIRE AMOUNT	----	LEAD COUNT	6	
MIN.PAD PITCH (mm)	----	TOTAL WIRE LENGTH (mm)		LEAD PITCH	0.65	mm
MIN.PAD OPENING (mm)	----	MAX. WIRE LENGTH (mm)	----	BODY SIZE	2X2	mm
WIRE MATERIAL		MIN. WIRE LENGTH (mm)	----	FLAG SIZE	1X1.7	mm
WIRE DIA. (mil)		SHEET	----	PLATING	DOUBLE RING	

Table 12 DFN-6 Pin Assignments

Pin	Name
1	VDD1
3	CC
4	VSS
6	VDD2
Other (2,5)	NC

Notes: Pin 1 marking and labeling information to come

9.0 REFERENCES

[1] USB 3.1 Type C specification, http://www.usb.org/developers/docs/

Available soon:

[2] indie e-marker reference design

[3] indie cable test board specification and programming information

10.0 REVISION HISTORY

Table 13 Revision History

Rev #	Date	Action	By
1.0		Original Obsidian spec 1.0	
1.0	6/18/2015	indie format and part number	CR
2.0	12/07/2015	Update on diagram, BoM and package	RH/CR
2.1	12/10/2015	Update contacts information	VW

11.0 ORDERING INFORMATION

Table 14 Ordering information

Order code	Description
iND80001-c1	USB Cable Marker in WCSP-4 package
iND80001-d1	USB Cable Marker in DFN-6 package
iND80001EVK_C1	Cable programming board [3]
iND80001SUP_C1	WCSP paddle reference design [2]

12.0 CONTACTS

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